

1                    **A SCAN BASED MULTIPLE RING OSCILLATOR STRUCTURE**  
2                    **FOR ON-CHIP SPEED MEASUREMENT**

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4                    **TECHNICAL FIELD**

5                    The technical field is tracking process variations.

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7                    **BACKGROUND ART**

8                    Ring oscillators are often used in analog parameter testing (APT) structures generated by wafer  
9 manufacturers. The manufacturer makes a wafer and different dies sit on the wafer. One important  
10 function is to try and optimize the number of dies placed on one wafer. To save space, manufacturers  
11 place the APT structures in the area between two dies.

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13                    Speed binning is usually done based upon some type of broadside test performed by a package  
14 tester. These tests are run by the fabrication which saves the information in a database. Due to the  
15 limitations of wafer testing, broadside speed testing is usually delayed until the dies are packaged. Thus,  
16 it is often difficult to know the speed of a part at wafer test. There are other ring oscillator structures  
17 placed on a chip to attempt to compensate for process variation, however, none of them export their  
18 information outside of the chip.

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20                    Furthermore, in prior applications, manufacturers "best guess" would be to add an extra five  
21 percent here or an extra ten percent here because they believe a particular thing is going to happen or  
22 they want to see what is going to occur in the system. This means that some method to get a "best  
23 guess" at the speed of the part at wafer test will significantly reduce the price of packaging a part that  
24 will not make the frequency cutoff. In addition, several processes make it easy to set the speed at  
25 wafer test and difficult to set at package test. Thus, there is a need to measure process variation at  
26 wafer, package and system test cycles.

## SUMMARY OF INVENTION

The present invention bundles four ring oscillators, a 20-bit ripple counter and the necessary control logic needed to implement a Joint Test Action Group (JTAG) scan based interface. The present system can be located on every die, so that each location can be individually tested. It communicates with the outside world through a standard JTAG interface. It is accessible at wafer, package, and system test which allows for several methods of correlating the oscillator speed to the speed of a part in the actual system.

Those skilled in the art will appreciate these and other advantages and benefits of various embodiments of the invention upon reading the following detailed description of a preferred embodiment with reference to the below-listed drawings.

## BRIEF DESCRIPTION OF DRAWINGS

Figure 1 is a diagram showing a scan based multiple ring oscillator structure; and

Figure 2 is a block diagram implementing the structure of Figure 1.

## DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

**Figure 1** illustrates a system 100 that tracks process variations. Circuit 117 includes read only scan latches 105 that contain four control bits. The function of the circuit is for clock and count control. The circuit 117 controls which one of the clocks is going to run. The four control bits of the scan latches are BIT 0 - OSCSELA, BIT 1 - OSCSELB, BIT 2 - RESET and BIT 3 - ENAB. In addition to the four control bits, the scan latches 105 also includes two inputs signals: SHIFT clock and SCAN IN, and an output signal SCAN OUT.

Circuit 121 includes scan chain 110 that contains 20 scan bits used to scan out a final count of a 20-bit counter 160. The function of circuit 121 is to count the clock and capture the count onto the

1 scan chain 110. The system 100 uses the SHIFT signal to transfer all the data into scan latches 105  
2 and out of the scan chain 110. By controlling the SCANIN signal in conjunction with the SHIFT  
3 signal, control bits can be loaded into the scan latches 105 or results readout from SCANOUT1 from  
4 scan chain 110. Reset circuitry exists to ensure that the manufacturer does not power on a chip with  
5 one of the oscillators 115 running.

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7 Circuit 119 selects one of the clocks to input to the 20-bit counter 160. Once the manufacturer  
8 uses the SHIFT and the SCAN IN signals to set OSCSELA and OSCSELB, multiplexer 120 will turn  
9 on the appropriate ring oscillator 115. If OSCSEL A0 and OSCSEL B0 are selected, RING oscillator  
10 125 will be enabled by the ENAB signal. If OSCSEL A0 and OSCSEL B1 are selected, LTRAN  
11 oscillator 130 will be enabled. If OSCSEL A1 and OSCSEL B0 are selected, RTRAN oscillator 135  
12 will be enabled. If OSCSEL A1 and OSCSEL B1 are selected, LVT oscillator 140 will be enabled.  
13 The oscillators 115 are built from FET structures. Each FET has a FET capacitor type load to allow  
14 a reasonable frequency with a low number of stages. By having two control bits select the oscillator,  
15 the manufacturer can run one and only one of the oscillators 115 at a time.

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17 The outputs of the RING oscillator 125 and the LTRAN oscillator 130 feeds into NOR gate  
18 145. The outputs of the RTRAN oscillator 135 and the LVT oscillator 140 feeds into NOR gate 150.  
19 The outputs of both the NOR gates 145 and 150 feed into a NAND gate 155. The output of the  
20 NAND gate 155 is an OSC signal which is the input to a 20-bit counter 160. The OSC signal is a  
21 clock signal. The counter 160 increments by one count every time the clock ticks. Once the  
22 manufacturer has the count they can run a READ signal 165 in the scan chain that transfers the number  
23 of times the selected oscillator toggled during the test time into the scan chain 110. Once in the scan  
24 chain 110, subsequent SHIFT clocks scan the number out through SCAN OUT1. Scanout and  
25 Scanin1 simply connect circuit 117 and circuit 121 to make one continuous scan chain. There can only  
26 be one input signal and one output signal for this to be considered a single chain. The other input to the  
27 20-bit counter 160 is the RESET signal from the read only scan latches 105. The RESET signal resets

1 the counter 160 to zero before powering. The counter 160 is a ripple counter with an asynchronous  
2 reset.

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4 **Figure 2** is a flow chart implementing the structure described in Figure 1. The system initially  
5 sets the RESET signal to be on (step 200). By controlling the SCAN IN signal and toggling the SHIFT  
6 clock this sets the RESET bit to be on. Next, the system selects and enables an oscillator (step 205).  
7 The manufacturer uses the SHIFT clock and SCANIN to set the proper bits in OSCSELA and  
8 OSCSELB and turn on the ENAB signal. In addition, the RESET bit is now turned off. In order to  
9 start count, the SHIFT clock is toggled once (step 210) and then the SHIFT clock is toggled again to  
10 stop the count (step 215). The time period between toggling the SHIFT clock on and toggling the  
11 SHIFT clock off indicates the test time. The first count is loaded in BIT 0 of the counter 160. The  
12 next count will move the value in BIT 0 to BIT 1 and place the new value into BIT 0. The toggling of  
13 the SHIFT clock will load up the counter 160. Once the counter is loaded, the READ signal is  
14 activated to transfer the count into the scan chain 110 (step 220). The SHIFT clock is toggled once  
15 more and the results of the scan in are read out of SCAN OUT1 (step 225). Next the designer decides  
16 if a new test needs to be conducted. If a new is conducted (step 230), the RESET bit is turned on.  
17 Otherwise, the system has completed the test (step 235).

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19 The present invention does not necessarily require any other control structures. The  
20 manufacturer does not have to actually be executing code on the CPU, rather all the manufacturer  
21 needs is access to the three pins to turn on the ring oscillator to count it, turn it off and then scan out the  
22 count and then do calculation and software to find out how fast it would work. JTAG accessibility and  
23 all of the control structure set up to use the JTAG functionality make it very usable.

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25 In the present invention, the system 100 enables manufactures to initially test the wafer before  
26 the dies are cut apart. This allows the manufactures to know of any defects on the wafer before cutting  
27 it apart. If there is a defect, the manufacturer does not cut up that particular wafer, however, upon  
28 testing, the wafer is good, the manufacturer cuts apart the wafer into separate dies. Now the

1 manufacturer can test each individual die prior to packaging. Thus, the present invention allows the  
2 manufacturer to have access at wafer, package or system test life cycle.

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4 By having access at the various test cycles, the sooner the manufacturer knows of the defect,  
5 the more money the manufacturer saves. If the manufacturer can find a defect at wafer, then the  
6 manufacturer does not have to put it into a package and spend hundreds of dollars to get into a package  
7 when they can throw it away immediately. Furthermore, if there is a way the manufacturer can put parts  
8 into a system and easily find out what the ring oscillator does in the system, what it does in the package  
9 test and what it does at wafer test, then the manufacturer can correlate that to how fast the manufacturer  
10 can actually run that part in the system. This information gives the manufacturer a real good focus on  
11 what they have to do to the wafer to be able to have the part run properly in the system. Therefore,  
12 it allows the manufacturer to take data in the system test and easily apply it back to the wafer test for  
13 manufacturing.

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15 The terms and descriptions used herein are set forth by way of illustration only and are not  
16 meant as limitations. Those skilled in the art will recognize that many variations are possible within the  
17 spirit and scope of the invention as defined in the following claims, and their equivalents, in which all  
18 terms are to be understood in their broadest possible sense unless otherwise indicated.

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20 What is claimed is:  
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